25.4 A 10b 205MS/s 1mm² 90nm CMOS Pipeline ADC for Flat-Panel Display Applications

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With the scaling down of CMOS technology, the increased unity-gain frequency and reduced device dimension promise the integration of multi-functional high-speed circuits with a smaller chip area and lower power consumption. However, the thin gate oxide and short channel length, usable only in low supply voltages, cause several disadvantages in analog circuit design, such as insufficient operating voltage margin in cascode circuits, switch linearity degradation, and low supply/substrate noise immunity. On the other hand, the next-generation analog flat-panel interface circuits include three 10b 205MS/s ADCs that deal with a $1.0V_{PP}$ single-ended input and can control the offset and gain of independent RGB or YGC signals under the noisy system environment. This work describes an ADC that employs several techniques to handle the design limitations in a 90nm process.

The proposed ADC consists of a core ADC, 2 DACs for gain and offset control, a regulator, and an input buffer. All stages of the core ADC use 3b multiplying DAC (MDAC) considering power consumption and linearity in Fig. 25.4.1. The second and third flash blocks that operate at opposite clock phases, share a reference resistor ladder to reduce the active area and power consumption. The 9b R-2R single-ended DAC generates 0.25 to 0.50V, the voltage difference between top and bottom nodes of reference resistor ladders that gives a 6dB gain variation to the ADC. The offset control is realized by the 8b binary-coded current-steering DAC and the offset control range is ±256mV. The 1.0V supply for the analog blocks of the core ADC is provided by the LDO regulator [1] to isolate the analog supply from external supply noise. The regulator can be selectively operated, so the analog supply is applied directly from off-chip when the regulator is off. The digital outputs are converted into low-voltage overlapped differential signals, driving off-chip 100Ω resisters, to facilitate high-speed digital capturing with low digital noise [2].

In this application, the input has a $1.0V_{PP}$ single-ended signal swing and around 100MHz bandwidth, conditions that make it difficult to achieve 10b level linearity at the sampling switch of a S/H circuit. Although clock boostrapping techniques can enhance the switch linearity, those techniques are contrary to the trend of a low gate breakdown voltage in sub-100nm CMOS processes. To guarantee high linearity without the boostrapping techniques, as illustrated in Fig. 25.4.2, a switched source follower is proposed in front of a S/H circuit instead of the sampling switch and the conventional source follower that has been used to drive the high-speed S/H circuit. In the switched source follower, the input signal leakage through the parasitic capacitors of the transistors MP_1 and MP_2 during the holding phase Q_2 of the S/H circuit deteriorates the linearity of the sampled signal, so the resistor-switch ladder at the input stage of the S/H circuit in Fig. 25.4.3 shorts the bottom plates of the sampling capacitors C_S and C_{SB} during the Q_2 phase to reduce the effect of the leakage.

The DC gain and transconductance of amplifiers, in low-voltage design, is more sensitive to supply and process variations because of the reduced drain-source saturation voltage that demands a higher DC gain and bandwidth in amplifier design. For a sufficiently high DC gain with a wide output swing, the front-end S/H circuit and first-stage MDACs have an additional amplifier stage compared to the conventional circuits. The S/H circuit uses a 2-stage amplifier as shown at the bottom of Fig. 25.4.3. The CMOS input pair of the second stage A_2 enhances the output swing with lower transconductance variation and reduces the power consumption compared to the conventional NMOS or PMOS input pair topology in which the reduced transconductance seriously degrades the phase margin for a large signal swing. In the bias circuit, the drain voltage of the bias transistor M_{CS3} is designed to have the same voltage as that of M_{CS2}, so the transistors can operate properly even in the deep linear region [3]. The first-stage MDAC uses a 3-stage amplifier with a reversed nested Miller-compensation topology [4]. The first stage of the 3-stage amplifier has a folded-cascode architecture with an NMOS input pair, and the second and third stages have the same common-source topology as the second stage of the S/H circuit.

Figure 25.4.4 shows the measured dynamic performance of the ADC with a varying input frequency at 205MS/s, and the peak SNDR is ~56dB for a $1.0V_{PP}$ differential signal at a low frequency. The SNDR of a $1.0V_{PP}$ single-ended input is lower than that of the differential input because of the third harmonic distortion caused by the front-end source follower, which is identified by comparing the SFDRs for the single-ended and differential inputs. An SFDR of more than 60dBc is achieved up to nearly 100MHz frequency for a $1.0V_{PP}$ single-ended input, and the input bandwidth could be improved by increasing the transistor size and current consumption of the source follower. For a 79MHz $1.0V_{PP}$ single-ended input, the SNDR is 53.9dB and the SFDR is 61.8dBc.

In the noisy system environment, the PSRR limits the dynamic performance of the ADC. To measure the PSRR for the external high-frequency supply noise separately from the supply noise caused by its own clock, the noise tone is applied through the bias tee, and the noise voltage is directly measured from the supply and ground pins of the test chip by the wide-bandwidth high-impedance active probe and spectrum analyzer as shown in Fig. 25.4.5(a). When the regulator operates, the PSRR is improved by more than 20dB for up to 200MHz supply noise compared to when the regulator does not operate. In Fig. 25.4.5(b), the PSRRs with and without the regulator are 53dB and 24dB, respectively, for 100MHz noise. Figure 25.4.5(c) shows the maximum achievable SNDR of an ideal 10b ADC calculated from the measured PSRR when 100MHz $100mV_{PP}$ noise is added to the analog supply. The maximum SNDR without a regulator is expected to be around 44dB and the measured value is 41.4dB. On the contrary, for the same level of supply noise, the measured SNDR with a regulator has < 0.2dB degradation compared to that of without noise.

The performance of the ADC is summarized in Fig. 25.4.6. The total power consumption of a single-channel ADC is 111mW for a 30MHz sinusoidal input signal at 205MS/s with the regulator operated at a 3.0V supply. The core ADC draws 40mA from a 1.0V supply, so when the regulator is not used and the analog supply is applied externally (off-chip), the total power consumption is ~61mW, including the input buffer and 21mW for the 2 DACs. The measured differential nonlinearity and integral nonlinearity are ±0.5LSB and ±0.5LSB, respectively, for a $1.0V_{PP}$ differential signal. The proposed ADC is implemented in a 90nm n-well CMOS process with an active area of 1.0mm² in Fig. 25.4.7.

References:

[1] G. A. Rincon-Mora, P. E. Allen, "A Low-Voltage, Low-Quiescent Current, Low Drop-Out Regulator," *IEEE J. Solid-State Circuits*, vol. 33, pp. 36-44, Jan., 1998.
[2] S.-C. Lee, K.-D. Kim, J.-K. Kwon, et al., "A 10-bit 400-MS/s 160-mW 0.13mm CMOS Dual-Channel Pipeline ADC Without Channel Mismatch Calibration," *IEEE J. Solid-State Circuits*, vol. 41, pp. 1596-1605, Jul., 2006.
[3] K. Gulati, H. S. Lee, "A High-Swing CMOS Telescopic Operational Amplifier," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2010-2019, Dec., 1998.
[4] R. Eschauzier, J. Huijsing, Frequency Compensation Techniques for Low-Power Operational Amplifiers, Boston, MA: Kluwer Academic, 1995.

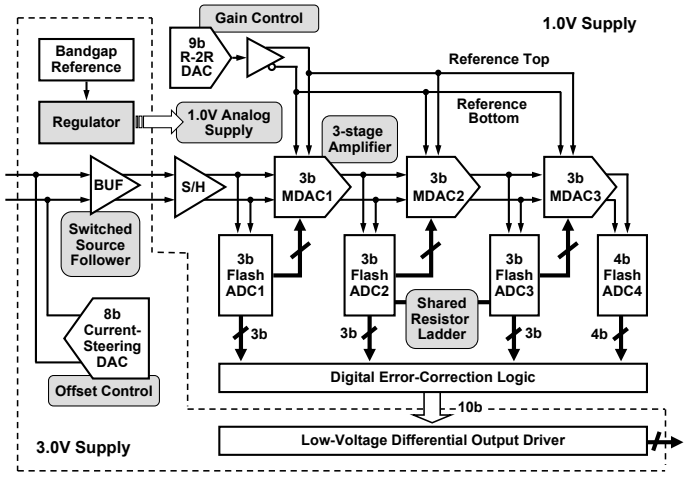


Figure 25.4.1: Block diagram of the proposed ADC.

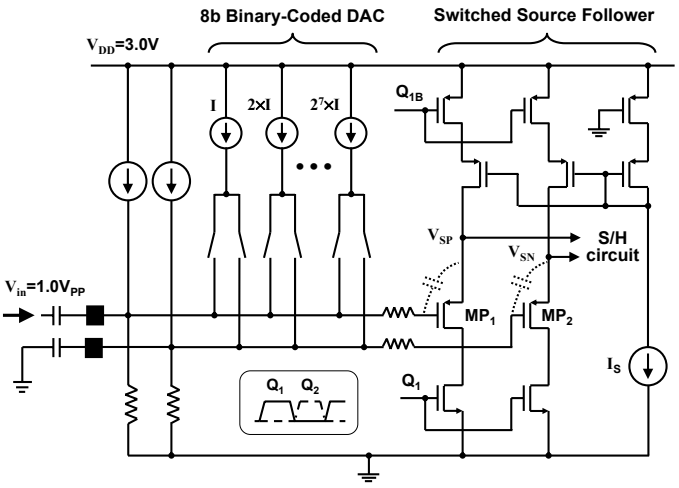


Figure 25.4.2: Switched source follower and offset-control circuit.

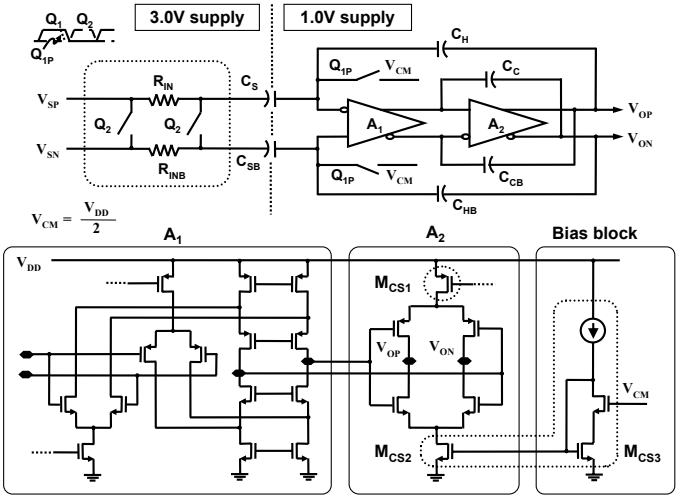
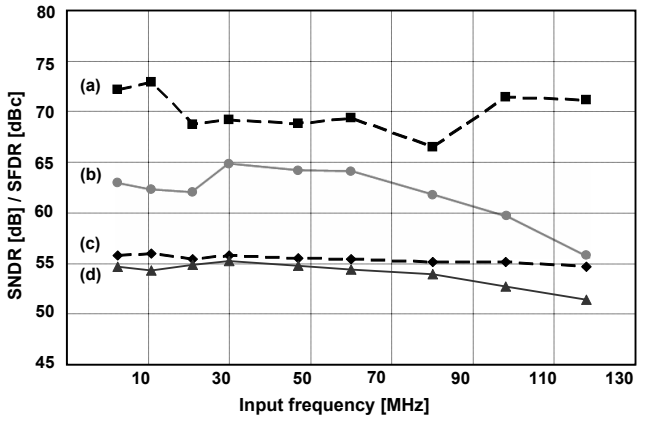


Figure 25.4.3: S/H circuit employing a 2-stage amplifier.



(a) SFDR of 1.0V_{PP} differential input. (b) SFDR of 1.0V_{PP} single-ended input.
(c) SNDR of 1.0V_{PP} differential input. (d) SNDR of 1.0V_{PP} single-ended input.

Figure 25.4.4: Dynamic performances versus input frequencies (f_s=205MS/s).

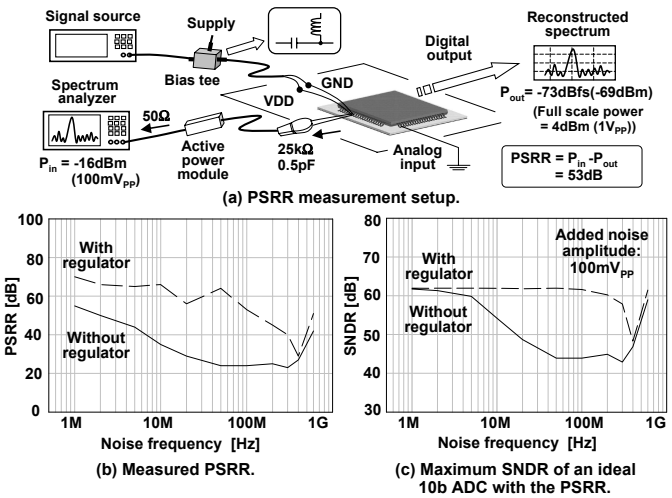


Figure 25.4.5: PSRR measurement.

Resolution		10b	
Sampling speed		205MS/s	
Input range		1.0V_{PP} (Single-ended)	
Power consumption		With regulator	Without regulator
		111mW	61mW
SNDR	f_{in}=30MHz	55.2dB	
	f_{in}=79MHz	53.9dB	
Active area (per channel)		1.0mm² (=1.3mm×0.8mm)	
Technology		90nm CMOS 1P6M	

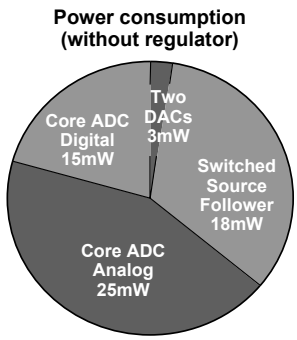


Figure 25.4.6: Performance summary.

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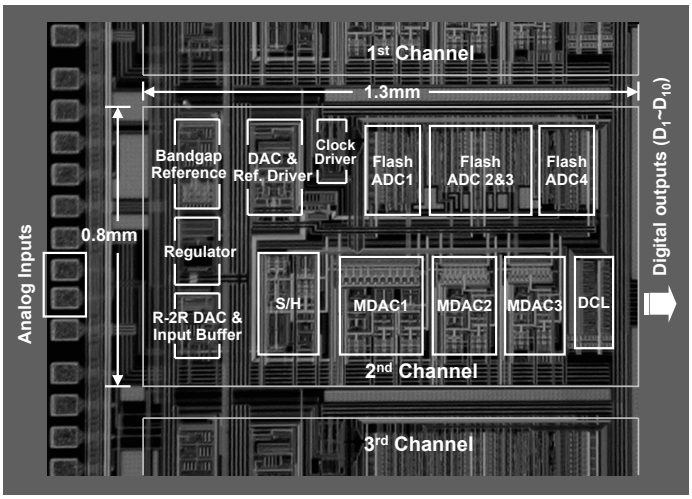

Figure 25.4.7: Die micrograph.

